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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/924,337	08/06/2001	Shunpei Yamazaki	07977-211003	3550

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EXAMINER	
NELSON, ALECIA DIANE	
ART UNIT	**PAPER NUMBER**
2675	

DATE MAILED: 02/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/924,337	YAMAZAKI ET AL.	
	Examiner	Art Unit	
	Alecia D. Nelson	2675	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14 and 16-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *20,25,33 and 34* is/are allowed.

6)☒ Claim(s) *1-14,16-19,21-24 and 26-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

2. ***Claims 1-14 and 22*** are rejected under 35 U.S. C. 103(a) as being unpatentable over Sasaki et al (U.S. Patent No. 5,818,068) in view of Funai et al. (U.S. Patent No. 5,550,070).

With reference to **claim 1,** Sasaki et al. plurality of pixels (82) arranged in a matrix including source lines and gate lines, driver circuitry (84, 85) for driving the source lines and the gate lines (66, 67), and a logic circuit for processing a signal required for driving the driver circuits (see column 6, lines 24-27), which are formed on the same insulating substrate (see column 5 lines 44-56), wherein the pixel matrix circuit, the driver circuit, and the logic circuit are constituted by a plurality of TFTs, each having an active layer comprising crystalline silicon (see column 6, lines 7-38). Further Sasaki et al. teaches that the TFT composed of the polycrystalline silicon film is formed in a manner that the directions in which the crystal grows are substantially parallel to a direction in which carriers in the film move (see column 11, line 66-column 12, line 10).

While Sasaki et al. teaches the usage of a logic circuit, there fails to be disclosure that the logic circuit includes at least on or more of the claimed components. However, it is disclosed that a logic circuit can be included as opposed to the shift register (61), wherein it is well known by those skilled in the art that a shift register can be considered a type of memory device (see column 20, line 61-column 21, line 4). Also, while Sasaki et al. teaches that the crystals grow in a substantially parallel direction, there is no disclosure that the crystals are rod-shaped, however such shape of liquid crystal are known to those skilled in the art.

Funai et al. teaches that the crystalline silicon region (108) is made of a plurality of needle-shaped or column-shaped silicon crystals having a growth

direction in parallel with the surface of the substrate (101) (see column 8, lines 55-58).

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to allow the crystal to be of rod, needle, or column-shape, as taught by Funai et al., and extending in one direction, as taught by Sasaki et al. and Funai et al. to be used in a system similar to that which is taught by Misawa and Sasaki et al. so that a leak current flowing between the shaped crystals becomes less and thereby further increasing the display characteristics and performance of the display device.

With reference to **claims 2-4,** Funai et al. further teaches that in the crystalline silicon film (110), the needle-shaped or column-shaped silicon crystals grow in a direction represented by an arrow (125), and in each needle-shaped or column-shaped silicon crystal, no grain boundaries are present in the direction (125) (see column 10, lines 11-15).

With reference to **claims 5 and 6,** it is an obvious function of liquid crystal devices for there to be an anisotropic property between the channel length direction and a channel width direction of the active layer, as well as there is and intrinsic or substantially intrinsic channel form region of the active layer.

With respects to **claims 7 and 8,** Sasaki et al. teaches that the metal element for enhancing crystallization includes at least one selected from the group consisting of nickel, iron, cobalt, palladium, and platinum. Sasaki et al. fails to teach the specific amount in usage, however the amount of metal element used is designers choice.

With reference to **claim 9,** Funai et al. teaches a gate insulating film (113) is formed on the crystalline silicon film (112), and a gate electrode (114) is formed on the gate insulating film (113). Further it is taught that in the case where the amorphous silicon film (103), the high-concentration nickel region (109), and the region (107) containing nickel in large concentrations are included in the crystalline silicon film (112) (see column 9, lines 45-62).

With respects to **claims 10 and 14,** the usage of plural TFT connecting to each picture element, and the usage of a phase compararator, low pass filter, ect, in a logic circuit, is well known in the art.

With respects to **claims 11-13,** Sasaki et al. teaches that the TFT circuit includes a mask layer (33) (see column 10, lines 50-65) and that the pixels include a pixel capacitance (111) and a hold capacitance (110) (see column 15, lines 9-33).

With reference to **claim 22,** Sasaki et al. teaches that the device could be an electroluminescence display device (see column 14, lines 41-54).

3. ***Claims 16, 17, 23 and 27-29*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Hush et al. (U.S. Patent No. 5,638,085) in view of Assaderaghi et al. (U.S. Patent No. 5,811,857).

With reference to claims 16, 17, 27 and 28 Hush et al. teaches a pixel matrix circuit (22); a driver circuit (46, 60) for driving the pixel circuit; and a logic circuit (33) for processing a signal required for driving the driver circuit; wherein the pixel circuit, the driver circuit and the logic circuit are formed over the same substrate (see column 4, lines 11-14) and constituted with a plurality of N-channel type thin film transistors and a plurality of P-channel thin film transistors (see column 13, lines 52-55), wherein the logic circuit includes a phase comparator (34), a low pass filter (38), a voltage controlled oscillator (42), a frequency divider (column 10, lines 44-49). With respect to the oscillator for the source and gate line driver, Hush et al. fails to teach this aspect of the limitation, however the usage of an oscillator with the line drivers are well known in the art.

While teaching the usage of the N and P type transistors, there is no disclosure of the subthreshold coefficient transistors being in a range of 60 to 100 mV/decade.

Assaderaghi et al. teaches the usage of N and P type transistors wherein the ideal subthreshold swing is 60 mV/decade (see column 5, lines 41-44).

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention for the TFT's having the subthreshold coefficient as taught by Assaderaghi et al. to be used in a device similar to that which is taught by Hush et al. in order to provide ideal characteristics for the TFT's of the active circuits of the display device.

With reference to **claims 27 and 29**, Hush teaches that the device is of electroluminescent type display device (see column 4, lines 21-28).

4. ***Claims 18, 19, 21, 24, 26, and 30-32*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Hush et al. in view of Sasaki et al.

Hush et al. teaches a pixel matrix circuit (22) including source lines and gate lines leading from the driver circuits; a driver circuit (46, 60) for driving the pixel circuit; and a logic circuit (33) for processing a signal required for driving the driver circuit and a signal including image information transmitted to the pixel matrix circuit; wherein the pixel circuit, the driver circuit and the logic circuit are formed over the same substrate (see column 4, lines 11-58) and constituted with a plurality of N-channel type thin film transistors and a plurality of P-channel thin film transistors (see column 13, lines 52-55), wherein the logic circuit includes at least one of a phase comparator (34), a low pass filter (38), a voltage controlled oscillator (42), a frequency divider (column 10, lines 44-49).

With respect to the oscillator for the source and gate line driver, Hush et al. fails to teach this aspect of the limitation, however the usage of an oscillator with

the line drivers are well known in the art. Further, while teaching that the power supply provides various potentials as needed for use by the TFT's circuits of the display (see column 4, lines 59-64), there fails to be any teachings of the dimensions of the TFT are made different based on required electrical characteristics. However, it would have been obvious for the TFT's of the active circuits to have different dimensions being that they each operate at different frequencies in order to reduce power consumption. Also, while teaching the active circuits are constituted by TFT's there are no teachings of each having an active layer comprising crystalline silicon.

Sasaki et al. teaches a pixel circuit (82), driver circuitry (84, 85) and a logic circuit (see column 6, lines 24-27) each having an active layer comprising crystalline silicon (see column 6, lines 7-38).

Therefore it would have been obvious to one having ordinary skill in the art at the time of the invention to allow for each of the TFT's of the active circuits to have an active layer comprising crystalline silicon as taught by Sasaki et al. to be used in a device similar to that which is taught by Hush et la. in order to thereby provide TFT circuits having improved characteristics, including higher operation speed, producing a display device with high display performance.

With reference to **claim 21**, Hush et al. teaches all that is required as explained above with reference to independent claims 18 and 30. Further, while teaching that the power supply provides various potentials as needed for use by the TFT's circuits of the display (see column 4, lines 59-64) and while teaching

that the pixel matrix circuit, driver circuits, and logic circuit includes two kinds of circuits (see Figures 1, 4, 6, and 7), there are no teachings of the two kinds of circuits being different from each other in at least one of a driving frequency and an operating voltage. However, as explained, with the power supply be designated to apply only the required operational voltages to the active circuits, it would therefore be obvious to one having ordinary skill in the art for the active circuits to apply only the necessary operational voltages to the circuits in order to reduce power consumption.

With reference to ***claims 24, 26, and 32*** Hush teaches that the device is of electroluminescent type display device (see column 4, lines 21-28), and is also taught by Sasaki et al. (see column 14, lines 50-54).

Allowable Subject Matter

5. ***Claims 20, 25, 33, and 34*** are allowed.

Response to Arguments

6. Applicant's arguments filed 10/04/04 have been fully considered but they are not persuasive.

With regards the rejection of **claim 1**, the applicant argues that the office action is unclear as to what elements of Sasaki are asserted to correspond to applicant's claimed "logic circuit", wherein Sasaki appears to fail to teach a logic circuit separately from the driver circuit(s) of the reference. However, this

rejection has been changed, and the arguments are thereby moot. Further, throughout the specification there are more teachings concerning the logic circuits of the device (see column 6, lines 24-38 and column 20, lines 61-column 21, line 4). Moreover nowhere in the claims is it stated that the logic circuit is separate from the driver circuits.

Applicant's arguments with respect to **claims 16-21 and 23-26** have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alecia D. Nelson whose telephone number is (703) 305-0143. The examiner can normally be reached on Monday-Friday 9:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (703) 306-0403. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

adn/ADN
February 18, 2005

AMR A. AWAD
PRIMARY EXAMINER

Amr Ahmed Awad